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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,509	10/12/2001	Richard L. Hudson	42390P11897	3993

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EXAMINER
ALI, SYED J

ART UNIT	PAPER NUMBER
2127	

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DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,509	HUDSON, RICHARD L.	
	Examiner	Art Unit	
	Syed J Ali	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are pending in this application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 3, 9, and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

4. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "CLI" in claims 3, 9, and 17 is used by the claim to mean "a programming language", while the accepted meaning is "an operating system." The term is indefinite because the specification does not clearly redefine the term.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. **Claims 1-6 and 18-22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.**

7. As per claim 1, the language of the claim raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment or machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101. The claimed "method" should be modified to indicate that it is embodied in a manner as to be executable, e.g. "a computerized method". Claims 2-6 are rejected for at least the same reasons as claim 1, as they fail to present any limitations that resolve the deficiencies of the claim from which they depend.

8. As per claim 18, the claimed "instruction set" is non-statutory for at least the reason that it is not tangibly embodied in a manner as to be executable. Claims 19-22 are rejected for at least the same reasons as claim 18, as they fail to present any limitations that resolve the deficiencies of the claim from which they depend.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. **Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Hudson et al. ("Cycles to Recycle: Garbage Collection on the IA-64").**

11. As per claims 1-4; Hudson teaches the invention as claimed, including a method comprising:

monitoring thread switches in a multiple-threaded application through use of a thread switch flag (§4.2.2, Fig. 3), wherein the multiple-threaded applications are supported by a computer programming language selected from the group consisting of Java, C#, CLI, LISP, and Pascal (Abstract);

executing a non-blocking thread synchronization sequence (§3, Fig. 14);

interrupting the non-blocking thread synchronization sequence upon the occurrence of a thread switch (§4.2.2, Figs. 3-4); and

repeating the non-blocking thread synchronization sequence (Fig. 3).

12. As per claims 5-6, Hudson teaches the invention as claimed, wherein the non-blocking thread synchronization sequence is a frontier pointer-based allocation sequence (§5), wherein executing the frontier pointer-based allocation sequence comprises:

loading a frontier pointer into a first register (§4.1);

moving a current value of the frontier pointer to a second register (§4.1);

adding the size of an object to be allocated to the first register such that a new frontier pointer is determined (§4.2.2);

storing a virtual method table to the second register if a thread switch has not occurred (§4.1); and

updating the frontier pointer with the new frontier pointer if a thread switch has not occurred (§4.1, §4.2.2).

13. As per claims 7-12, Hudson teaches the invention as claimed, including a machine-readable medium that provides executable instructions, which when executed by a processor, cause the processor to perform the method of claims 1-6, respectively (§4.2.2).

14. As per claim 13, Hudson teaches the invention as claimed, including a computing system comprising:

at least one central processing unit, the central processing unit executing multi-threaded applications (§4.2.2);

a thread switch indicator to indicate the occurrence of a thread switch (§4.2.2, Fig. 3); and

an instruction set to implement non-blocking thread synchronization sequences such that partially completed non-blocking thread synchronization sequences used to share resources local to the at least one central processing unit can be abandoned and repeated upon the occurrence of a thread switch (§4.2.2, Figs. 3-4).

15. As per claim 14, Hudson teaches the invention as claimed, including the computing system of claim 13 wherein the instruction set includes:

a set instruction to set the thread switch indicator upon the occurrence of a thread switch (§4.2.2, Fig. 3);

a first conditional move instruction to move data if the thread switch indicator is set (Fig. 3);

a second conditional move instruction to move data if the thread switch indicator is not set (Fig. 3);

a first jump instruction to bypass instructions if the thread switch indicator is set (§4.2.2);

a second jump instruction to bypass instructions if the thread switch indicator is not set (§4.2.2); and

a clear instruction to clear the thread switch indicator (Fig. 3).

16. As per claim 15, Hudson teaches the invention as claimed, including the computing system of claim 14 wherein the thread switch indicator is a thread switch flag (§4.2.2, Fig. 3).

17. As per claim 16, Hudson teaches the invention as claimed, including the computing system of claim 13 wherein each of the at least one central processing units has a single allocation area (§4.2.2) and the non-blocking thread synchronization sequence is a frontier pointer-based allocation sequence (§5).

18. As per claim 17, Hudson teaches the invention as claimed, including the computing system of claim 13, wherein the computing system uses a computer programming language selected from the group consisting of Java, C#, CLI, LISP, and Pascal (Abstract).

19. As per claims 18, Hudson teaches the invention as claimed, including a computer instruction set comprising:

a thread switch indicator to indicate the occurrence of a thread switch (§4.2.2, Fig. 3);

a set instruction to set the thread switch indicator upon the occurrence of a thread switch (§4.2.2, Fig. 3);

a first conditional move instruction to move data if the thread switch indicator is set (Fig. 3);

a second conditional move instruction to move data if the thread switch indicator is not set (Fig. 3);

a first jump instruction to bypass instructions if the thread switch indicator is set (§4.2.2);

a second jump instruction to bypass instructions if the thread switch indicator is not set (§4.2.2); and

a clear instruction to clear the thread switch indicator (Fig. 3).

20. As per claim 19, Hudson teaches the invention as claimed, including the computer system instruction set of claim 18 implemented as hardware (§4.8).

21. As per claim 20, Hudson teaches the invention as claimed, including the computer system instruction set of claim 18 wherein the thread switch indicator is a thread switch flag (§4.2.2, Fig. 3).

22. As per claim 21, Hudson teaches the invention as claimed, including the computer system instruction set of claim 18 used to implement a non-blocking thread synchronization sequence for the execution of multi-threaded applications (§3, Fig. 14).

23. As per claim 22, Hudson teaches the invention as claimed, including the computer system instruction set of claim 21 wherein the non-blocking thread synchronization sequence is a frontier pointer-based allocation sequence (§5).

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J Ali whose telephone number is (571) 272-3769. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Syed Ali
February 10, 2005

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